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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,275	11/18/2003	Jae-Kwon Choi	10125/4131	6054

7590 10/18/2006

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EXAMINER	
SHENG, TOM V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,275	CHOI, JAE-KWON	
	Examiner	Art Unit	
	Tom V. Sheng	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *1-3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-19* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show each of the signals separately as described in the specification. Specifically, fig. 5, 6, 8 and 9 are all captures of digital oscilloscope, the signals being cramped together making it difficult to differentiate between them. Moreover, fig. 5 and 8 are not provided with any references. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 4-6 are objected to because of the following informalities: the reset circuit in claim 4 actually includes the elements of the filtering circuit, as clearly described in the specification (paragraphs 37-38). The elements related to the filtering circuit should be defined accordingly with respect to the filtering circuit in the claim. Appropriate correction is required. Claims 5 and 6 are dependent on claim 4.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 9 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 9, lines 1-2, it is unclear to one of ordinary skill in the art as to how to make use of the invention since the mere citing of first, second and third resistors and a transistor would not allow one to construct the filtering circuit.

As for claim 10, lines 1-2, it is unclear to one of ordinary skill in the art as to how to make use of the invention since the claim limitation merely cites the well known components in a bipolar transistor without defining any connection between the transistor and the resistors. Claims 10-14 are dependent on claim 9.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7, 8 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koga et al. (US 6,894,673), hereinafter Koga, in view of Admitted Prior Art.

As for claim 7, Koga teaches a liquid crystal display device, comprising:

a LCD module (liquid crystal display 2; fig. 6) including a gate driver (gate driver 23) and a source driver (source driver 22; column 8 lines 1-15);

a timing controller (LCD control circuit 1) supplying a gate operation enable (GOE - gate driver output enable signal VOE) signal to the gate driver (gate driver 23) and a clock signal (data latch pulse DLP) to the source driver (source driver 22; column 8 lines 1-23 and 60-67);

a reset circuit (rise detection circuit 11 with NOR gate 12; fig. 9 - incorporated into control circuit 1) supplying a reset signal (signal HRST) to the timing controller (specifically to horizontal counter 13 and maximum value detection circuit 15), the reset signal enabling the GOE signal (within frame HRST is determined by rise detection circuit 11 and between frames HRST is determined by maximum value detection circuit 15, coincidence detection circuit 16 and tx setting circuit 17; see column 10 line 22 through column 11 line 7); and

a filtering circuit (maximum value detection circuit 15, coincidence detection circuit 16 and tx setting circuit 17 - incorporated into control circuit 1) connected to the reset circuit (output from coincidence detection circuit 16 is connected an input of NOR gate 12), the filtering circuit permitting a GOE mask time of the GOE signal (the duration of the VOE signal between frames is determined by the tx value detected; see column 11 lines 8-26) and reducing an impulse of the clock signal (during inter-frame time, the VOE causes VCK and corresponding DLP to shift/delay, thus eliminating an undesirable DLP pulse that would occur if there is no provision of the VOE signal; see fig. 7 and column 9 lines 1-33). For complete details, see fig. 6-10 and column 7, line 51 through column 11, line 54.

However, Koga does not teach the timing controller including an electrostatic protection circuit and that the GOE mask time of GOE signal to be longer than about 16 msec. Admitted Prior Art teaches the use of electrostatic protection circuit 28 at an input data terminal of the timing controller 22 (fig. 2; pages 5-7). Inherently, by setting the LVDS voltage between DVCC and ground by means of two serially connected diodes, variation in voltages due to electrostatic is limited. Moreover, even though Koga does not teach any specific VOE mask time minimum, it is understood that the minimum time is to be set according to factors such as frame rate, color depth, display resolution, etc.

Therefore, it would have been obvious to one of ordinary skill in the art to incorporate an electrostatic protection circuit (and with data transmission in LVDS form)

and to further set a minimum VOE mask duration, in order to provide optimal display by equalizing charging times of all lines of pixels and minimizing electrostatic spikes.

As for claim 8, APA teaches that power supply voltage DVCC is connected to one end of the EPC 28 and ground is connected to the other end (see fig. 2). However, APA and Koga do not teach DVCC being applied to the filtering circuit (i.e. the circuits 15-17 as analyzed above). On the other hand, one of ordinary skill in the art would recognize the basic need of a power supply voltage to a circuit to provide power and/or a reference level for operation. Therefore, it would have been obvious to provide either a digital or analog VCC (a power supply voltage) because the provision would provide the necessary power supply and/or also a reference level to the circuits 15-17 for operation.

As for claim 15, APA teaches that before power is supplied to DVCC, there is an induced voltage of about 0.3v to about 0.7v at DVCC, and when power is supplied, the DVCC is at 3.3v. See fig. 2-4 and paragraphs 9-12 of the specification.

Claims 16-19 are rejected similarly per rejection analyses of claim 7. Specifically, claimed operation signal, timing signal, additional signal correspond to Koga's gate driver output enable signal VOE to the gate driver, data latch pulse DLP to the data driver, and signal HRST, respectively.

7. Claims 7, 8 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (JP 11-249613), in view of Admitted Prior Art.

As for claim 7, Shin teaches a liquid crystal display device (child display 5; fig. 1), comprising:

a LCD module (LCD 20) including a gate driver (inherent) and a source driver (inherent);

a timing controller (mask processing circuit 30 with PLL circuit 23) supplying a gate operation enable (ENB2) signal to the gate driver and a clock signal (DCLK1) to the source driver;

a reset circuit (IC 21) supplying a reset signal (ENB1) to the timing controller (mask processing circuit 30), the reset signal enabling the GOE signal (ENB2 is enabled when ENB1 is active; see paragraphs 30 and 31); and

a filtering circuit (inverter 40 with flip-flop 43 and AND circuit 44, which are part of circuit 30) connected to the reset circuit (as shown), the filtering circuit permitting a GOE mask time of the GOE signal (MASK signal) and reducing an impulse of the clock signal (between t1 and t2, MASK signal is low thus masking the turbulence section of ENB1, resulting in an inactive ENB2 until tb; see fig. 2, 3 and paragraphs 34-41).

However, Shin does not teach the timing controller including an electrostatic protection circuit and that the GOE mask time of GOE signal to be longer than about 16 msec. Admitted Prior Art teaches the use of electrostatic protection circuit at the input data terminal of the timing controller 22 (fig. 2; pages 5-7). Inherently, by setting the LVDS voltage between DVCC and ground by means of two serially connected diodes, variation in voltages due to electrostatic is limited. Moreover, even though Shin does

not teach any specific ENB2 mask/inactive time minimum, it is understood that the minimum time is to be set according to various display requirements.

Therefore, it would have been obvious to one of ordinary skill in the art to incorporate an electrostatic protection circuit (and with data transmission in LVDS form already shown between IC 14 and IC 21) and to further set a minimum MASK duration, in order to provide optimal display by removing display errors due to signal turbulence when ENB1 becomes active.

As for claim 8, APA teaches that power supply voltage DVCC is connected to one end of the EPC 28 and ground is connected to the other end (see fig. 2). However, APA and Shin do not teach DVCC being applied to the filtering circuit (i.e. inverter 40 with flip-flop 43 and AND circuit 44 as analyzed above). On the other hand, one of ordinary skill in the art would recognize the basic need of a power supply voltage to a circuit to provide power and/or a reference level for operation. Therefore, it would have been obvious to provide either a digital or analog VCC (a power supply voltage) because the provision would provide the necessary power supply and/or also a reference level to the inverter 40 with flip-flop 43 and AND circuit 44 for operation.

As for claim 15, APA teaches that before power is supplied to DVCC, there is an induced voltage of about 0.3v to about 0.7v at DVCC, and when power is supplied, the DVCC is at 3.3v. See fig. 2-4 and paragraphs 9-12 of the specification.

Claims 16-19 are rejected similarly per rejection analyses of claim 7. Specifically, claimed operation signal, timing signal, additional signal correspond to Shin's ENB2 to the gate driver, DCLK1 to the data driver, and ENB1, respectively.

Allowable Subject Matter

8. Claims 4-6 are objected, but would be allowed upon corrections.

9. Claims 11-14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: none of the prior arts of record teaches "a transistor including an emitter connected to a first node, a base connected to a second node and a collector connected to a third node, a digital input voltage (DVCC) being applied to the first node; a first resistor connected between the first and second nodes; a second resistor connected between the second node and a fourth node, the fourth node being grounded; a third resistor connected between the third and fourth nodes; a fourth resistor connected between the third node and a fifth node, the fifth node being connected to the at least one input terminal; and a capacitor including a first electrode connected to the fifth node and a second electrode that is grounded" of claim 4, and "wherein a first end of the first resistor is connected to the emitter, a second end of the first transistor and a first end of the second transistor are connected to the base, a first end of the third resistor is connected to the collector, a second end of the second resistor and a second end of the third resistor are grounded, and the DVCC is applied to the emitter" of claim 11. Claims 5-6 and 12-14 are dependent on claims 4 and 11, respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V. Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tom Sheng
September 26, 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER